REMARKS

Procedural History of Case

The above-identified patent application is currently under final rejection. Applicant is submitting with this Reply a Request for Continued Examination under 37 C.F.R. § 1.114. In light of this Request for Continued Examination, applicant understands that the finality of the rejection is considered withdrawn.

Summary of Office Action

Claims 3-43 were pending in the above-identified patent application.

The Examiner rejected claims 3, 7, 8, 18, 21-23, 27, 28, 30-32, 34, 37, and 42-43 under 35 U.S.C. § 102(b) as being anticipated by Riley, Jr. U.S. Patent 4,272,729. Claims 19 and 20 were rejected under 35 U.S.C. § 103(a) as being obvious from Riley in view of Berry et al. U.S. patent 6,366,174. Claims 33, 35, 36, and 38-41 were rejected under 35 U.S.C. § 103(a) as being obvious from Jefferson U.S. Patent 5,744,991 in view of Riley. Each of claims 4-6, 9-17, 24-26, and 29 was objected to as depending from a rejected base claim, but allowable subject matter was indicated.

Summary of Applicant's Reply

Applicant notes with appreciation the indication of allowable subject matter in claims 4-6, 9-17, 24-26 and 29, and hereby expressly reserves the right to rewrite any one or more of those claims in independent form should the base claims ultimately not be allowed.

Applicant has canceled claim 22 without prejudice and amended claims 3-6, 23-26, 42, and 43 to more particularly define the invention. The claims are fully supported by the specification as filed and no new subject matter has been added.

The Examiner's rejections and objection are respectfully traversed.

Applicant's Reply to the Rejections of
Claims 3, 7, 8, 18-23, 27, 28, and 30-43

Claims 3, 7, 8, 18, 21-23, 27, 28, 30-32, 34, 37, 42, and 43 were rejected under 35 U.S.C. § 102(b) as being anticipated by Riley. Claims 19 and 20 were rejected under 35 U.S.C. § 103(a) as being obvious from Riley in view of Berry. Claims 33, 35, 36, and 38-41 were rejected under 35 U.S.C. § 103(a) as being obvious from Jefferson in view of Riley. The Examiner's rejections are respectfully traversed.

Applicant's invention, as defined by amended independent claims 3 and 23, relate to a loop circuit that includes a compensation component, a high-gain coarse feedback path, and a low-gain fine feedback path. Claim 3 relates to a phase-locked loop circuit, while claim 23 relates to a delay-locked loop circuit. The coarse feedback path includes a high-gain signal modifier downstream of either a frequency detector (in the case of claim 3) or a phase detector (in the case of claim 23), the high-gain signal modifier having a first gain. In addition, the fine feedback path includes a low-gain signal modifier downstream of either a phase-frequency detector (in the case of claim 3) or a phase detector (in the case of claim 23), the low-gain signal modifier having a second gain that is less than the first gain. The references cited by the Examiner, whether taken singly or combination, neither show nor suggest these features of applicant's claims 3 and 23.

The high-gain signal modifier of the coarse feedback path and the low-gain signal modifier of the fine feedback path of applicant's invention provide substantial immunity to noise, without substantially narrowing the frequency range within which the loop circuit can operate. Applicant's specification explains:

> [The fine feedback] path operates at a relatively low gain, so that signal noise (e.g., a power supply variation) will not cause a large phase or frequency variation in the loop circuit output. Despite the lower gain of this fine feedback path, the loop circuit of the invention, as a whole, retains a wide operating range as a result of the inclusion as well of the aforementioned coarse feedback path. As stated above, the component

> contributed by the coarse feedback path becomes fixed before the loop circuit is locked, so that notwithstanding the high gain of the coarse feedback path, voltage variations in the coarse feedback path are not multiplied by the high gain of that path to distort the loop circuit. Page 8, lines 8-21.

An illustrative example of such signal modifiers is shown in FIG. 2. As explained in applicant's specification, page 10, lines 35-37, voltage-to-current converter 21 has a relatively high gain, while voltage-to-current converter 22 has a relatively low gain.

In contrast, FIG. 1 of Riley shows a frequency synthesizer 10 and a coarse tuning circuit 24. The Examiner contends that successive approximation register 30 is a high-gain signal modifier, as defined by applicant's independent claims 3 and 23. Applicant respectfully disagrees. As explained in the specification of Riley,

> [Successive] approximation register 30 includes a digital register which stores a digital number. Depending on the sense of the frequency error of the divided oscillator output signal, i.e., whether the output signal from the frequency detector 26 is high or low, the successive approximation register 30 algebraically adds bit weightings to adjust the value of the digital number stored in its register successively from the most significant bit to the least significant bit. Col. 4, line 62 to col. 5, line 3.

Thus, successive approximation register 30 maintains a digital number that indicates the direction and magnitude of a detected frequency error. Nowhere does Riley show or suggest a high-gain signal modifier in the coarse feedback path downstream of either a frequency detector or a phase detector, the high-gain signal modifier having a first gain, as defined by applicant's claims 3 and 23, respectively.

In addition, the Examiner contends that switch 44 of Riley is a low-gain signal modifier, as defined by applicant's independent claims 3 and 23. Applicant respectfully disagrees. Riley states:

> The switch 44 can be actuated to switch the phase-locked loop error voltage to its nominal center value in response to production of the START

> command signal by the switch 36, for example. Thereafter, the switch 44 can reconnect the fine tune control input terminal of the voltage controlled oscillator 12 to the output terminal of the loop filter 22 when the successive approximation register 30 produces an output signal indicating that the successive approximation process has completed. Col. 6, lines 20-28.

In other words, switch 44 of Riley initializes frequency synthesizer 10 at startup and enables fine tuning upon completion of the successive approximation process. Nowhere does Riley show or suggest a fine feedback path including a low-gain signal modifier downstream of either a phase-frequency detector or a phase detector, the low-gain signal modifier having a second gain that is less than the first gain, as defined by applicant's claims 3 and 23, respectively.

The remaining references do not make up the deficiencies of Riley in failing to show or suggest the claimed phase-frequency detector in a fine feedback path. Berry is cited only for its disclosure of counters in phase-locked loops, while Jefferson is cited only for its disclosure of processing circuitry incorporating a loop circuit. Accordingly, even combining Riley with either or both of Berry and Jefferson would not show the claimed invention.

For at least the reasons set forth above, applicant respectfully submits that independent claims 3 and 23 are allowable. Accordingly, dependent claims 7, 8, 18-21, 27, 28, and 30-43 are also patentable. Applicant respectfully requests that the rejections to claims 3, 7, 8, 18-21, 23, 27, 28, and 30-43 be withdrawn.

Applicant's Reply to the Objection of Claims 4-6, 9-17, 24-26, and 29

For at least the reasons set forth above, applicant respectfully submits that independent claims 3 and 23 are patentable. Accordingly, each of dependent claims 4-6, 9-17, 24-26, and 29 should also be patentable.

Conclusion

For the reasons set forth above, applicant respectfully submits that this application is in condition for allowance. Reconsideration and prompt allowance of this application are respectfully requested.

Respectfully submitted,

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